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09/894,205	06/28/2001	Kazushi Kurata	10873.753US01	7105

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EXAMINER	
GERSTL, SHANE F	

ART UNIT	PAPER NUMBER
2183	5

DATE MAILED: 06/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/894,205	Applicant(s) KURATA, KAZUSHI
	Examiner Shane F Gerstl	Art Unit 2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06/28/01, 10/09/07, and 02/23/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *3, 4, 7, 8, 11, 12, 15, and 16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,6,9,10,13,14 and 17-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-24* are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3 and 4*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *6* .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 2, 5, 6, 9, 10, 13, 14, and 17-24 have been examined.

Papers Received

2. Receipt is acknowledged of priority and both information disclosure statement papers submitted, where the papers have been placed of record in the file.

Election/Restrictions

3. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1, 2, 5, 6, 9, 10, 13, 14, and 17-24, drawn to a data processing device, classified in class 712, subclass 226.

II. Claims 3, 4, 7, 8, 11, 12, 15, and 16, drawn to a program conversion device, classified in class 717, subclass 140.

The inventions are distinct, each from the other because of the following reasons:

4. Inventions I and II are related as subcombinations disclosed as usable together in a single combination. The brief summary shows that the data processing device of group I and the program conversion device of group II are usable together. Page 3, line 28 – page 4, line 14 describe the data processing device. Page 4, line 17 – page 5, line 1 describe the program conversion device. Page 4, lines 28-31 and page 4, line 35 – page 5, line 1 show that the program conversion device creates a program suitable for use with the data processing apparatus. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention I has separate utility such as shown on pages 4-5 of the application. Page 4, lines 28-31 and page 4, line 35 – page 5, line 1 show that it is *possible* to obtain a machine level

program using the program conversion device that is suitable for use in the data processing device, clearly showing that it is not required that the program be used for only the data processing device of the current invention but one of ordinary skill in the art would recognize that other processors would be able to execute the program given by the program conversion device. These points are subsequently shown with the other embodiments as well. Thus, the data processing device can be used without the program conversion device. See MPEP § 806.05(d).

5. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

6. Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

7. During a telephone conversation with Douglas P. Mueller on 17 May 2004 a provisional election was made with traverse to prosecute the invention of Group I, claims 1, 2, 5, 6, 9, 10, 13, 14, and 17-24. Affirmation of this election must be made by applicant in replying to this Office action. Claims 3, 4, 7, 8, 11, 12, 15, and 16 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Specification

8. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is

requested in correcting any errors of which applicant may become aware in the specification.

9. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: DATA PROCESSING DEVICE THAT EXECUTES COMMAND INSTRUCTIONS WHICH DETERMINE IF INSTRUCTIONS SUBSEQUENT AND ASSOCIATED WITH CONDITIONAL INSTRUCTIONS MEET THE CONDITION AND IF NOT ARE OVERRIDDEN.

Drawings

10. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the command instruction being prior to the subsequent instructions in the instruction memory and instruction sequence must be shown or the feature(s) canceled from the claims. No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

11. Claims 18, 20, 22, and 24 are objected to because of the following informalities: A claim which depends from a dependent claim should not be separated by any claim which does not also depend from said dependent claim. It should be kept in mind that a

dependent claim may refer to any preceding independent claim. In general, applicant's sequence will not be changed. See MPEP § 608.01(n).

Appropriate correction is required.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. Claims 1, 2, 5, 6, 9, 10, 13, 14, and 17-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Cocke (3,577,189).

14. In regard to claim 1, Cocke discloses a data processing device reading in and executing instructions in a certain sequence, the data processing device comprising:

a. a fetch portion for reading in a computational instruction; Figure 1 shows that instruction address are sent to an external storage or instruction memory for fetching as outlined in column 11, lines 65-69. Table III of column 4 shows that two conditional branch instructions (a first and second conditional instruction) are executed along with an Exit instruction. Column 2, lines 2-9 show that the exit instruction is the point where control to a target instruction transferred (computed) and thus the exit instruction is a computational instruction and is also fetched from this memory.

b. a decoding portion for decoding the computational instruction that has been read in; Figure 1A, element 40 illustrates an instruction decoder that

decodes instructions as shown in column 2, lines 49-51 and thus the computational instruction is also decoded by this portion.

c. an execution portion for executing the decoded computational instruction; Column 2, lines 20-27 show that instructions are processed (executed) including the exit (computational) instruction. This is inherently done by an instruction processing, or execution, portion of the processor.

d. and an instruction overriding control circuit that overrides, of one or a plurality of subsequent instructions that follow the computational instruction in said sequence and are associated with the computational instruction, all but one of the subsequent instructions, in accordance with an execution result of the computational instruction. Column 3, line 73 – column 4, line 16 show that multiway branches (branches that point to different code sections) are processed with a single exit instruction that chooses, based on the conditions, the appropriate subsequent instruction to transfer control to (target instructions from the first or second branch) where the other subsequent instruction is overridden since it is not executed. The computational (exit) instruction is executed prior to the subsequent instructions since it must be executed before control is transferred to the appropriate following subsequent instructions. This is all inherently done in some sort of circuit, which is appropriately named an instruction overriding control circuit due to its function.

15. In regard to claim 2, Cocke discloses the data processing device according to claim 1, wherein said one or plurality of subsequent instructions is a subsequent

instruction group including a plurality of instruction strings. As shown in figure 7, the subsequent instructions after the exit instruction are a string of multiple instructions or a plurality of shorter instruction strings (such as a string of two instructions).

16. In regard to claim 5, Cocke discloses a data processing device reading in and executing instructions in a certain sequence (column 1, line 74 – column 2, line 2), the data processing device comprising an instruction memory (figure 1 shows a line 113 that sends an instruction address to external storage or an instruction memory), a fetch portion (column 11, lines 65-69), a decoding portion (figure 1A, element 40), an instruction execution portion, and an instruction overriding control portion (as shown below);

a. wherein the instruction memory stores a first subsequent instruction corresponding to a first conditional instruction from which the first condition has been eliminated, a second subsequent instruction corresponding to a second conditional instruction from which the second condition has been eliminated, and a command instruction that is arranged prior to the first subsequent instruction and the second subsequent instruction in the instruction sequence, and that indicates that the first subsequent instruction and the second subsequent instruction have contradictory execution conditions, and that indicates the contradictory execution conditions generated from the first condition and the second condition; Table III of column 4 shows that two conditional branch instructions (a first and second conditional instruction) are executed along with an Exit instruction. Column 2, lines 2-9 show that the exit instruction is the point

where control to a target instruction transferred. Column 3, line 73 – column 4, line 16 show that multiway branches (branches that point to different code sections) are processed with a single exit instruction that chooses, based on the conditions, the appropriate subsequent instructions to transfer control to (target instructions from the first or second branch) where the other set of subsequent instructions are overridden since they are not executed. Since one or the other of the branch paths are taken and not both the conditions are contradictory and the exit point is a command instruction. Also, since the exit instruction bases its decision on the conditions of the conditional instructions (branches) the conditions have been resolved or eliminated before the command instruction is analyzed as described in column 2, lines 20-21 where the exit is detected after condition determination. Finally, since instruction fetching is done from external storage or memory (as shown in figure 1), the instructions are inherently stored in this memory and the command (exit) instruction is stored prior to the subsequent instructions since it must be executed before control is transferred to the appropriate subsequent instructions.

b. wherein the fetch portion fetches the command instruction from the instruction memory; Figure 1 shows that instruction address are sent to an external storage or instruction memory for fetching as outlined in column 11, lines 65-69 and thus the command instruction is also fetched from this memory.

c. wherein the decoding portion decodes the fetched command instruction; Figure 1A, element 40 illustrates an instruction decoder that decodes instructions

as shown in column 2, lines 49-51 and thus the command instruction is also decoded by this portion.

d. wherein the instruction execution portion executes the decoded command instruction; Column 2, lines 20-27 show that instructions are processed (executed) including the exit (command) instruction. This is inherently done by an instruction processing, or execution, portion of the processor.

e. and wherein the instruction overriding control portion checks the execution result of the instruction command to determine which of the first condition and the second condition is satisfied, and overrides the instruction of the first subsequent instruction and the second subsequent instruction for which the condition is not satisfied, as shown above.

17. In regard to claim 6, Cocke discloses the data processing device according to claim 5, wherein the first conditional instruction, the second conditional instruction, the first subsequent instruction and the second subsequent instruction each consist of one instruction or an instruction group including a plurality of instruction strings. As shown above and in figure 7, the conditional instructions are one instruction (a branch) and the subsequent instructions (taken and overridden) are a string of multiple instructions or a plurality of shorter instruction strings (such as a string of two instructions).

18. In regard to claim 9, Cocke discloses a data processing device reading in and executing instructions in a certain sequence, the data processing device comprising:

a. a fetch portion for reading in a computational instruction; Figure 1 shows that instruction address are sent to an external storage or instruction memory for

fetching as outlined in column 11, lines 65-69. Table III of column 4 shows that two conditional branch instructions (a first and second conditional instruction) are executed along with an Exit instruction. Column 2, lines 2-9 show that the exit instruction is the point where control to a target instruction transferred (computed) and thus the exit instruction is a computational instruction and is also fetched from this memory.

b. a decoding portion for decoding the computational instruction that has been read in; Figure 1A, element 40 illustrates an instruction decoder that decodes instructions as shown in column 2, lines 49-51 and thus the computational instruction is also decoded by this portion.

c. an execution portion for executing the decoded computational instruction; Column 2, lines 20-27 show that instructions are processed (executed) including the exit (computational) instruction. This is inherently done by an instruction processing, or execution, portion of the processor.

d. and an instruction overriding control circuit which decides, in accordance with an execution result of the computational instruction, whether to override a subsequent instruction that follows the computational instruction in said sequence and is associated with the computational instruction, and which overrides this subsequent instruction in accordance with that decision. Column 3, line 73 – column 4, line 16 show that multiway branches (branches that point to different code sections) are processed with a single exit instruction that chooses, based on the conditions, the appropriate subsequent instruction to

transfer control to (target instructions from the first or second branch) where the other subsequent instruction is overridden since it is not executed. This is all inherently done in some sort of circuit, which is appropriately named an instruction overriding control circuit due to its function.

19. In regard to claim 10, Cocke discloses the data processing device according to claim 9, wherein said subsequent instruction is a subsequent instruction group including a plurality of instruction strings. As shown in figure 7, the subsequent instructions after the exit instruction are a string of multiple instructions or a plurality of shorter instruction strings (such as a string of two instructions).

20. In regard to claim 13, Cocke discloses a data processing device reading in and executing instructions in a certain sequence, the data processing device comprising an instruction memory, a fetch portion, a decoding portion, an instruction execution portion, and an instruction overriding control portion,

a. wherein the instruction memory stores a subsequent instruction corresponding to a conditional instruction from which the condition has been eliminated, and a subsequent execution condition command instruction that is arranged prior to the subsequent instruction in the instruction sequence, and that indicates that the subsequent instruction has an execution condition, and that indicates that execution condition; Table III of column 4 shows that two conditional branch instructions (a first and second conditional instruction) are executed along with an Exit instruction. Column 2, lines 2-9 show that the exit instruction is the point where control to a target instruction transferred. Column

3, line 73 – column 4, line 16 show that multiway branches (branches that point to different code sections) are processed with a single exit instruction that chooses, based on the conditions, the appropriate subsequent instructions to transfer control to (target instructions from the first or second branch) where the other set of subsequent instructions are overridden since they are not executed. Since one or the other of the branch paths are taken and not both the conditions are contradictory and the exit point is a command instruction. Also, since the exit instruction bases its decision on the conditions of the conditional instructions (branches) the conditions have been resolved or eliminated before the command instruction is analyzed as described in column 2, lines 20-21 where the exit is detected after condition determination. Finally, since instruction fetching is done from external storage or memory (as shown in figure 1), the instructions are inherently stored in this memory and the command (exit) instruction is stored prior to the subsequent instructions since it must be executed before control is transferred to the appropriate subsequent instructions.

b. wherein the fetch portion fetches the subsequent execution condition command instruction from the instruction memory; Figure 1 shows that instruction address are sent to an external storage or instruction memory for fetching as outlined in column 11, lines 65-69 and thus the command instruction is also fetched from this memory.

c. wherein the decoding portion decodes the fetched subsequent execution condition command instruction; Figure 1A, element 40 illustrates an instruction

decoder that decodes instructions as shown in column 2, lines 49-51 and thus the command instruction is also decoded by this portion.

d. wherein the instruction execution portion executes the decoded subsequent execution condition command instruction; Column 2, lines 20-27 show that instructions are processed (executed) including the exit (command) instruction. This is inherently done by an instruction processing, or execution, portion of the processor.

e. and wherein the instruction overriding control portion checks the execution result of the subsequent execution condition command instruction to determine whether the execution condition is satisfied, and overrides the subsequent instruction if the condition is not satisfied, as shown above.

21. In regard to claim 14, Cocke discloses the data processing device according to claim 13, wherein the conditional instruction and the subsequent instruction each include an instruction group including a plurality of instruction strings. As shown above and in figure 7, the conditional instructions are one instruction (a branch) and the subsequent instructions are a string of multiple instructions or a plurality of shorter instruction strings (such as a string of two instructions).

22. In regard to claim 17, Cocke discloses a data processing device according to claim 1, wherein the instruction overriding control portion lets the fetch portion skip the reading in of the subsequent instruction that is overridden. As shown above, a branch target path is overridden and another is taken. This means that the taken path will be next fetched for execution and the overridden will not be.

23. In regard to claim 18, Cocke discloses a data processing device according to claim 2, wherein the instruction overriding control portion lets the fetch portion skip the reading in of the subsequent instruction that is overridden. As shown above, a branch target path is overridden and another is taken. This means that the taken path will be next fetched for execution and the overridden will not be.

24. In regard to claim 19, Cocke discloses a data processing device according to claim 5, wherein the instruction overriding control portion lets the fetch portion skip the reading in of the subsequent instruction that is overridden. As shown above, a branch target path is overridden and another is taken. This means that the taken path will be next fetched for execution and the overridden will not be.

25. In regard to claim 20, Cocke discloses a data processing device according to claim 6, wherein the instruction overriding control portion lets the fetch portion skip the reading in of the subsequent instruction that is overridden. As shown above, a branch target path is overridden and another is taken. This means that the taken path will be next fetched for execution and the overridden will not be.

26. In regard to claim 21, Cocke discloses a data processing device according to claim 9, wherein the instruction overriding control portion lets the fetch portion skip the reading in of the subsequent instruction that is overridden. As shown above, a branch target path is overridden and another is taken. This means that the taken path will be next fetched for execution and the overridden will not be.

27. In regard to claim 22, Cocke discloses a data processing device according to claim 10, wherein the instruction overriding control portion lets the fetch portion skip the

reading in of the subsequent instruction that is overridden. As shown above, a branch target path is overridden and another is taken. This means that the taken path will be next fetched for execution and the overridden will not be.

28. In regard to claim 23, Cocke discloses a data processing device according to claim 13, wherein the instruction overriding control portion lets the fetch portion skip the reading in of the subsequent instruction that is overridden. As shown above, a branch target path is overridden and another is taken. This means that the taken path will be next fetched for execution and the overridden will not be.

29. In regard to claim 24, Cocke discloses a data processing device according to claim 14, wherein the instruction overriding control portion lets the fetch portion skip the reading in of the subsequent instruction that is overridden. As shown above, a branch target path is overridden and another is taken. This means that the taken path will be next fetched for execution and the overridden will not be.

Conclusion

30. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

31. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents have been cited to further show the art with respect to conditional instruction execution in general.

US Pat No 4,539,635 to Boddie teaches execution of a conditional instruction for disabling or overriding sections of execution.

US Pat 3,577,190 to Cocke discloses a skip instruction that overrides subsequent instructions based on a condition and thus a conditional instruction.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (703)305-7305. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703)305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane F Gerstl
Examiner
Art Unit 2183

SFG
May 20, 2004

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